Advanced Memory Optimization Techniques for Low-Power Embedded Processors

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The design of embedded systems warrants a new perspective because of the following two reasons: Firstly, slow and energy inefficient memory hierarchies have already become the bottleneck of the embedded systems. It is documented in the literature as the memory wall problem. Secondly, the software running on the contemporary embedded devices is becoming increasingly complex. It is also well understood that no silver bullet exists to solve the memory wall problem. Therefore, this book explores a collaborative approach by proposing novel memory hierarchies and software optimization techniques for the optimal utilization of these memory hierarchies. Linking memory architecture design with memory-architecture aware compilation results in fast, energy-efficient and timing predictable memory accesses. The evaluation of the optimization techniques using real-life benchmarks for a single processor system, a multiprocessor system-on-chip (SoC) and for a digital signal processor system, reports significant reductions in the energy consumption and performance improvement of these systems. The book presents a wide range of optimizations, progressively increasing in the complexity of analysis and of memory hierarchies. The final chapter covers optimization techniques for applications consisting of multiple processes found in most modern embedded devices. Advanced Memory Optimization Techniques for Low Power Embedded Processors is designed for researchers, complier writers and embedded system designers / architects who wish to optimize the energy and performance characteristics of the memory subsystem.

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